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Method of ultra fast MRAM write operation

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This summary report gives experts in the field an overview for an informed judgment about this pending patent (Priority application No.: EP05000667, priority date 14/01/2005). Besides this technical report, the Appendix A contains the exact phrasing of the claims in English language. Appendix B contains a list of references.

Introduction

Magnetic random access memories (MRAM) have the potential to capture a large part of the semiconductor memory market as they combine key features like

- non-volatility,
- low power consumption,
- unlimited write endurance,
- high speed of operation.

Most major semiconductor manufacturers are involved in research and development of MRAM devices. First market roll out is announced for 2005.

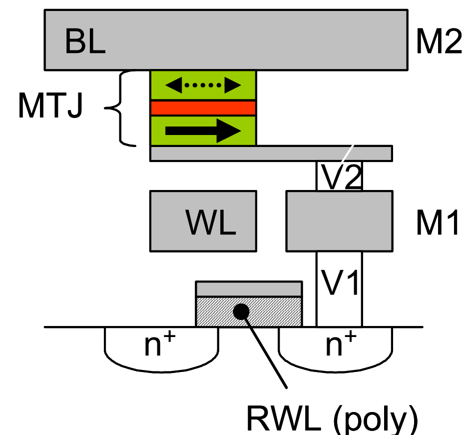

FIGURE 1: Schematic intersection a typical MRAM bit: The digital information is stored in the free layer magnetization of the magnetic tunnelling junction cell (MTJ). Read and write operation is performed through Bit line (BL). Perpendicular oriented write word line (WL) and and poly-Si read word line (RWL) are also shown.

A basic text-book like description of MRAM operation is given through Fig.1: In MRAMs the digital information is stored in the magnetization orientation of a magnetic tunnel junction cell (MTJ). An MTJ cells basically consists of two thin ferromagnetic layers (green) coupled by a tunneling oxide layer (red). The relative orientation of the magnetization (arrows) of the two ferromagnetic layers determines the digital memory state of the bit. Generally, the magnetization of one layer (the so-called pinned layer, fat arrow) is fixed by coupling to an antiferromagnet. The magnetization of the second ferromagnetic layer (the so-called free layer, dotted arrow) is either oriented parallel or antiparallel to the pinned layer magnetization. Switching of the free layer magnetization from parallel to antiparallel alignment changes the tunnelling magneto resistance (TMR) by about 50% thereby allowing read-out of the digital memory state.

MRAM read operation of the bit state is performed by passing a read-out current through the MTJ cell via the bit line (BL) and the selection transistor which is gated by the poly-silicon read word line (RWL). MRAM write operation is performed by passing currents through the magnetic field generation lines (BL,WL). The superposed magnetic field pulses generated by the bit line (BL) and the write word line (WL) are sufficient to switch the free layer magnetization and thus to program the cell into the two digital memory states.

Technical challenge and inventive solution

This invention solves the problem of magnetic excitation in ultra fast MRAM write operation. Magnetic ringing during and after writing operation through a magnetic field pulse is a known problem in these devices. Currently write fields must be applied for a duration of considerably above 2 ns to stabilize the written memory state. Consequently, the MRAM write clock rate is limited to values below 500 MHz.

The present invention solves the problem of magnetization ringing during MRAM write operation. The effect is achieved by optimization of the device geometry and by adapting the pulse parameters to the duration of the magnetization precession of the free layer during bit addressing. As a result reliable MRAM write operation by pulses shorter than 500 ps and thus ultra high MRAM write clock rates above 2 GHz is possible.

Further advantageous effects of the invention are a reduced write power consumption, a reduced heat load to the cells, and a reduced error rate during MRAM write operation.

The invention is protected by claims to a method of magnetization reversal, claims to a magnetic memory device and claims to a method of optimizing the switching parameters for a magnetic memory cell array.

Working Group and Inventor

The PTB is the German National Metrology Institute, dedicated by German federal law to determine the SI -units in ultra high precision and rivaled by very few world wide.

The invention is part of the research efforts of Department 2.5 *Semiconductor Physics and Magnetism*, lead by Dr. U. Siegner, to develop electronic devices, which can serve as quantum standards for the units of electrical resistance and electrical current. For the reproduction of electrical currents semiconductor circuits are developed in which single charge quanta can be manipulated. In the field of magnetism, the unit of magnetic flux density is realized and disseminated to customers from around the world by various calibration services. The Department 2.5 operates an internationally agreed reference laboratory for magnetic data storage media and develops measurement techniques for novel nanoscale magnetic materials that will form the magnetic storage media of the future.

Dr. Schumacher is working in Section 2.53 *Low dimensional Electron Systems* , which routinely grows low-dimensional semiconductor structures in a dedicated molecular beam epitaxy machine that the department operates in PTB´s clean room center. His present research activities are in the field of ultra fast magnetization dynamics and quantum transport phenomena in nano scale semiconductor devices.

Dr. Hans Werner Schumacher is one of the pioneers in the field of ultra fast precessional magnetization reversal in MRAMs. One of his scientific achievements was the experimental demonstration of the fastest ever realized magnetization reversal process in an MRAM cell prototype [1,2]. The measured switching time of only 165 ps of this so-called ballistic magnetization reversal represents the fundamental ultra fast physical limit of magnetization switching speed.

A further outcome of the research activities in the field of ultra fast magnetization dynamics was the first demonstration of coherent suppression of magnetization ringing in MRAM prototype cells [3].

Both experiments can be seen as major milestones towards ultra fast MRAM operation according to the invention.

Reliable simulations were also used to simulate and test the effects of ultra fast MRAM write operation of the present invention.

Problem of the Prior Art

In present MRAM prototypes reliable write operation is performed by pulses of at least 5 ns duration. The fastest write operation of a completed MRAM prototype reported so far was achieved on a device specially adapted for fast pulse propagation. On this device the minimum duration of the bit and word line pulses for reliable programming was 2.5 ns [4]. For shorter pulse durations an intolerable increase of the write error rate was found. The corresponding maximum MRAM write clock rate was well below 400 MHz.

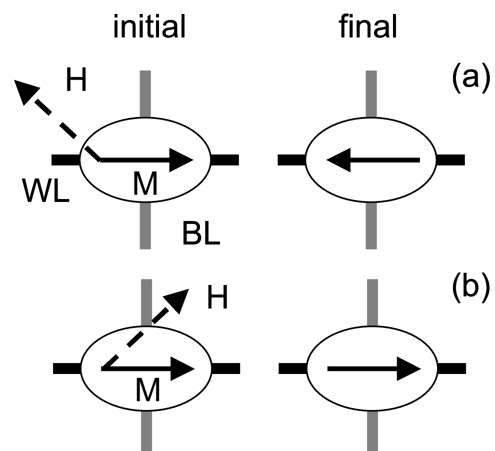

FIGURE 2: The two relative orientations of magnetic field H and cell magnetization M during write operation of an MRAM. In (a) the initial and final digital memory state during write operation differ. The applied field and the magnetization have an antiparallel component. In (b) the initial and final digital memory state during write operation are the same. The applied field and the magnetization have a parallel component.

The rather long pulse durations above 2 ns for reliable MRAM operation are due to the precessional motion of the free layer magnetization upon magnetic field pulse application. During writing of a cell in an MRAM array two basic relative field orientations of the initial cell magnetization M and the applied magnetic field pulse H occur. The two field orientations are sketched in Figure 2. During bit addressing of a cell in a standard MRAM array the magnetic field pulse H generated by the word and bit line is tilted with respect to the initial magnetization M.

The two cases differ in the orientation of the easy axis field component with respect to the initial magnetization M and in the effect on the magnetization state after write operation:

(a) the field pulse H has an antiparallel easy axis component and the magnetization M switches;

(b) the field pulse H has a parallel easy axis component and the magnetization M does not switch.

Both cases are characterized by different magnetization trajectories. The measured time evolution of two exemplary trajectories is shown in Figure 3. (a) shows the trajectory for switching. The magnetization switches within 400 ps (arrow) by performing a half precessional turn about the pulse field. In (b) the magnetization does not switch. However, the write pulse induces strong precessional excitations of the free layer magnetization [5]. Depending on the material and field pulse parameters these excitations persist for at least 1.5 to 5 ns.

For reliable prior art bit addressing the write pulses must thus be longer than the decay time of the precessional excitations in any cell of the MRAM array. The MRAM bit addressing time is thus limited to values above 2 ns. Consequently, MRAM write clock rates above 500 MHz are impossible.

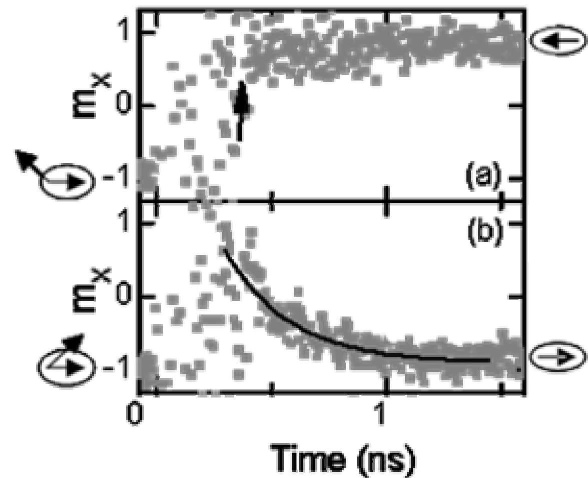

FIGURE 3: Measured magnetization trajectories for the two relevant cases of bit addressing. (a) Switching by antiparallel easy axis field component. The magnetization switches within less than 500 ps to the reversed orientation. **(b) non-switching by parallel easy axis field component**. The relaxation of the magnetization back to the initial orientation takes about 1.5 ns. This slow decay of magnetic excitations limits MRAM performance in prior art MRAM bit addressing.

Technical Details of the Invention

The MRAM write operation according to the invention leads to suppression of magnetic excitations due to field pulse application in any cell of the MRAM cell matrix. Thereby reliable MRAM write operation with write pulse durations well below 500 ps is achieved. The corresponding obtainable MRAM write clock rates are thus well above 2 GHz.

The concept of the invention is based on the simultaneous adaptation of the pulse parameters *for switching and for non-switching* to the time scale of the underlying magnetization precession of the free layer. To achieve ultra fast MRAM write operation the pulses are simultaneously tailored such that

(a) during **switching** the magnetization performs a **half precessional turn** about the applied field pulse;

(b) during **non-switching** the magnetization performs a **full precessional turn** about the applied field pulse.

In case (a) the magnetization switches by performing a half precessional turn about the applied field. After a half precessional turn the magnetization is in the reversed equilibrium orientation and thus in the new stable state. Consequently no magnetic excitations upon field pulse decay occur and the switched state is immediately stabilized.

In case (b) the magnetization performs a full precessional turn about the applied field. After a full precessional turn the magnetization is not reversed. Furthermore the magnetization is oriented very near the initial equilibrium orientation. Consequently, also here practically no magnetic excitations occur and the non-switched state is immediately stabilized.

Simulations of the magnetization dynamics with realistic pulse and device parameters show that it is possible to obtain both cases (a) and (b) simultaneously in MRAM arrays when properly adapting the field pulse parameters. A most advantageous mode of write operation is obtained when programming a set of memory cells (i.e. a "word") simultaneously. The obtainable write clock rates are then above 2 GHz per word and thus of *several GHz per bit*.

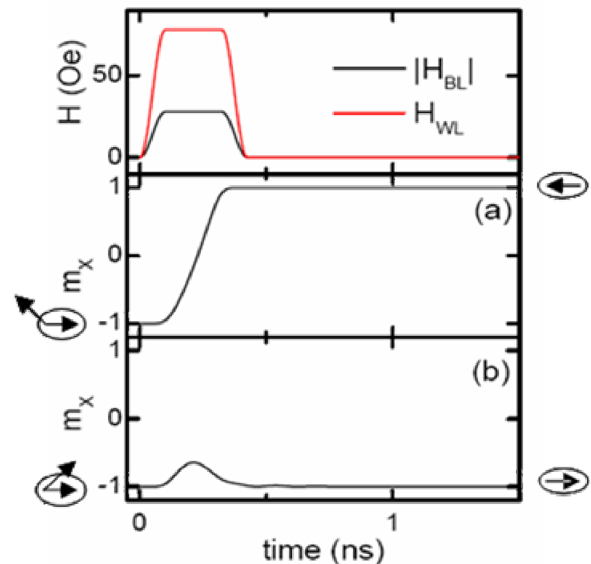

FIGURE 4: Bit and word line field pulses and magnetization trajectories according to one embodiment of the invention. The bit addressing pulses are shown in the upper panel. The bit write pulse duration is 325 ps (measured at half maximum). In both cases of switching (a) and non-switching (b) magnetization ringing upon field pulse decay is practically fully suppressed. The bit addressing is stabilized within less than 500 ps. Ultra high MRAM write clock rates above 2 GHz are possible.

Ultra fast bit addressing according to this embodiment of the invention can be obtained in a standard MRAM crossed wire write line architecture (cp. Figures 1,2). Figure 4 shows an example of optimized magnetization trajectories for such a device. In the example bit addressing is achieved by 325 ps bit/word line pulses. As seen in Figure 4 (a),(b) ringing upon field pulse decay is suppressed and switching *and* non-switching is stabilized within less than 500 ps. Note, that ringing is also suppressed for *all half select cells* (not shown).

Ultra high MRAM write clock rates above 2 GHz are thus possible.

In a further embodiment of the invention and ultra fast bit addressing is achieved in a novel MRAM architecture using hard axis field pulses, only. In the latter the MRAM is operated in a toggle write mode. The invention further discloses a step-by-step method to optimized MRAM bit addressing pulse parameters to allow ultra fast bit addressing for a given MRAM device.

Prototype Development

Presently, an ultra fast magnetization dynamics experiment is set up in the Section 2.5 of the PTB. The experiment allows the detection of the picosecond dynamics of MRAM cell prototypes using ultra fast magneto transport measurements. First results of the transport experiments are expected in autumn 2005. First experimental realization of ultra fast ("ballistic") bit addressing according to the invention are scheduled for the end of this year.

The research activities on ultra fast MRAM operation can be extended to involve industrial partners. If interested in joint research activities on ultra fast MRAM operation or in ultra fast operation testing of advanced MRAM prototypes please contact Dr. Schumacher, who should also be addressed for detailed technical questions.

Licensing

Comercial and other information on licensing policy are available through Dr. Bernhard Smandek at the Technology Transfer office of the PTB-Braunschweig.

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APPENDIX A:

Patent Claims

Claims

1. Method of magnetization reversal of the magnetization (M) of at least one first magnetic memory a element of an array of magnetic memory elements comprising the steps of:

- applying a first magnetic field pulse to a first set of magnetic memory elements, and

- applying a second magnetic field pulse to a second set of magnetic memory elements,

such that during the application of the first and second magnetic field pulse the magnetization (M) of said first magnetic memory element which is to be reversed upon the field pulse decay performs approximately an odd number of a half precessional turn,

characterized in
that the magnetization (M) of at least one second magnetic memory element which is not to be reversed upon the field pulse decay performs approximately an even number of a full precessional turn.

2. Method according to claim 1, characterized in

that the first and second magnetic field pulses are designed such that the first and second magnetic field pulses induce a full precessional turn of the magnetization (M) of a free layer (FL) of a corresponding magnetic memory element
and such that the superposition of at least the first and second field pulse induces a half precessional turn of the magnetization (M) of the free layer (FL) which reverses the magnetization (M) of the free layer (FL) of the selected magnetic memory element.

3. Method according to one of the preceding claims,
characterized in

programming a set of magnetic memory elements at the same time by applying a plurality of first and second magnetic field pulses to the array of magnetic memory elements, wherein the magnetic field pulses are applied such that the magnetization (M) of the magnetic memory elements which are to be reversed performs a half precessional turn during field pulse application and the magnetization (M) of the magnetic memory elements which are not to be reversed performs a full precessional turn during the magnetic field pulse application.

4. Method according to one of the preceding claims,
characterized in

that the precession period ($T_{prec}(H_{NS})$)of the magnetization (M) under application of an magnetic field pulse (H_{NS})which does not reverse the magnetization (M) of the magnetic memory element approximately matches the half of the precession period ($1/2\ T_{prec}(H_S)$) of the magnetization (M) under application of an effective magnetic field pulse (H_S) which does reverse the magnetization (M) of the magnetic memory element.

5. Method according to claim 4, characterized in
that the precession period mismatch

$$\Delta T = 1/2\ T_{prec}(H_S) - T_{prec}(H_{NS})$$

being the difference between the half of the duration of said first precession period ($1/2\ T_{prec}(H_S)$) and the duration of said full precession period $T_{prec}(H_{NS})$ is shorter than 100 ps ($\Delta T < 100$ ps).

6. Method according to one of the preceding claims,
characterized in

that the pulse duration of the field pulses for reversing the magnetization (M) and/or for non reversing the magnetization (M) are approximately matched to the duration of the half precession period at the field (Hs) which induces magnetization reversal.

7. Method according to one of the preceding claims,
characterized in

that the magnetic field pulses are oriented perpendicular to the initial and final easy axis of magnetization (M) of the magnetic memory elements of the array.

8. Method according to one of the preceding claims, characterized in that the applied magnetic field pulses have the same amplitude ($H_{HS,BL} = H_{HS,WL} = H_{HS}$) and the same pulse duration ($T_{HS,BL} = T_{HS,WL} = T_{HS}$).

9. Method according to one of the preceding claims, characterized in that the half precessional turn is in the range of 140° to 260° and/or that the full precessional turn is in the range of 320° to 400° about the effective magnetic field (H_{eff}) applied to the respective magnetic memory element.

10. Method for optimizing the switching parameters of a set of magnetic memory elements in an array of magnetic memory elements comprising by:
- determining the precession period $T_{prec}1$ of a first magnetic memory element of an array of magnetic memory elements upon application of, a first magnetic field pulse (H1),
- determining the precession period $T_{prec}2$ of a second magnetic memory element of an array of magnetic memory elements upon application of a second magnetic field pulse H2
- determining the precession period mismatch

$\Delta T = 1/2\ T_{prec}1 - T_{prec}2)$

being the difference between the half of the duration of the first precession period (1/2 $T_{prec}1$) upon application of the first magnetic field pulse (H1) and the duration of the full precession period ($T_{prec}2$) upon application of the second magnetic field pulse (H2), and
- determining the parameters for the first and second magnetic field pulses (H1, H2) for which the precession period mismatch is shorter than 100 ps ($\Delta T < 100$ ps).

11. Magnetic memory device comprising a set of first and second conductive lines and an array of a plurality of magnetic memory elements, each magnetic memory element having an easy axis of magnetization (M) and being situated in the vicinity of a respective meeting point of one of said first conductive lines (BL) and one of said second conductive lines (WL) for generating an magnetic field (H) at the respective magnetic element, wherein said second conductive line (WL) is aligned parallel to the easy axis of magnetization (M) of said magnetic memory element and the first conductive line (BL) is aligned perpendicular to the easy axis of magnetization (M) of said magnetic memory element in the vicinity of said magnetic memory element,
characterized by means for applying a set of first electrical pulses simultaneously to a plurality of first conductive lines (BL) and also simultaneously at least one second electrical pulse to at least one of said set of second conductive lines (WL), wherein the pulse duration is less than 10 ns.

12. Magnetic memory device comprising an array of a plurality of magnetic memory elements each magnetic memory element having an easy axis of magnetization (M), the memory device comprising a first conductive line (BL) for generating a magnetic field at at least one magnetic memory element, a second conductive line (WL) for generating a second magnetic field at the at least one magnetic memory element,
characterized in that said first and second conductive lines (BL, WL) having a parallel segment in the vicinity of the magnetic memory element, wherein the parallel segment of the first and second conductive lines (BL, WL) is oriented parallel to the easy axis of magnetization (M) of the magnetic memory element.

13. Magnetic memory device according to claim 11 or 12,
characterized in that the magnetic memory elements comprise at least one magnetic free layer (FL) comprising of a first ferromagnetic layer having a magnetic anisotropy (H_K), wherein the first ferromagnetic layer of the magnetic free layer (FL) further comprises a defined easy axis of magnetization and a distribution of the magnetization (M), said magnetization (M) being mainly oriented along the defined easy axis directions in equilibrium conditions.

14. Magnetic memory device according to one of the claims 11 to 13, characterized in that the free layer (FL) comprises a second ferromagnetic layer, wherein the average magnetization (M) of the second ferromagnetic layer of the free layer (FL) is oriented antiparallel to the orientation of the average magnetization (M) of the first ferromagnetic layer in equilibrium conditions.

15. Magnetic memory device according to one of the claims 11 to 14, characterized in that the free layer (FL) comprises a non-magnetic coupling layer between the first ferromagnetic layer and the second ferromagnetic layer.

Appendix B:

References

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